REMARKS/ARGUMENT

Claims 21-24, and 26-54 are pending after entry of this Amendment. No claim amendments are submitted. New claims 42-54 are submitted for examination.

Rejections under 35 U.S.C. §103

Claims 21, and 36-40 were rejected under 35 U.S.C. §103(a) as being unpatentable over Parikh (U.S. Patent No. 6,225,207) in view of Yu et al. (U.S. Patent No. 6,187,663). This rejection is traversed, and Applicants request reconsideration in view of the following argument.

The present invention, as described and illustrated by Applicants, and subsequently claimed in independent claim 21, claims a multi-layer dielectric layer over a substrate for use in dual-damascene applications. The multi-layer dielectric layer includes a barrier layer disposed over the substrate, an inorganic dielectric layer having a dielectric constant of about 4 disposed over the barrier layer, and a low dielectric constant layer disposed directly over the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

In independent claim 36, Applicants claim a dielectric structure for dual-damascene applications. The dielectric structure includes a barrier disposed over a base dielectric, an inorganic dielectric layer of a fluorine doped oxide disposed over the barrier, and a low dielectric constant layer of a carbon doped oxide disposed directly over, and in direct contact with, the inorganic dielectric layer. The low dielectric constant layer is configured to receive metallization line trenches to define a metallization line layer, and the inorganic dielectric layer is configured to receive vias during a dual-damascene process.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the

reference or to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art references when combined must teach or suggest all the claim limitations. (MPEP §2143). Applicants respectfully submit the Office has failed to establish a prima facie case of obviousness.

Parikh teaches methods for triple and quadruple damascene fabrication. According to the Parikh reference, triple damascene structures are fabricated in multiple consecutive "dielectric" layers. In one of Parikh's embodiments, two of the five layers are in fact etch stop layers. In other embodiments, at least three dielectric layers are disclosed to form the triple and quadriple damascene structures. The Parikh structures are fabricated using two etching sequences to form a power line trench, two signal line trenches, and vias. The power line trench, signal line trenches, and vias are filled to form triple and quadruple damascene structures.

The patent to Yu et al. teach a method for fabricating a copper damascene structure which includes two composite low-k dielectric layers each fabricated of two layers of low-k materials, and the two composite layers are separated by an etch stop layer of silicon oxynitride.

According to the Office in Paper 17, page 2, "layer 712 of fig 7F defines conductive path, signal line 752, to the substrate 710; layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being contact with the conductive path 752."

In Figure 7F, layer 710 is identified as substrate 710 (col. 12, line 38). Signal line 752 is described as "having an underlying via plug 754 which contacts substrate 710" (col. 13, lines 10-11). The reference itself discloses layer 712 is a first dielectric layer, "A first dielectric layer 712 is deposited on a substrate" (col. 12, lines 37-38). Layer 712 is *not* a barrier layer. The Office appears to be asserting that if *a portion* of the reference structure acts as a barrier, then the reference structure teaches a barrier. The Office fails to identify what the barrier is blocking, protecting, or otherwise serving as a barrier for or against. According to paper 17, "layer 712 functions as a barrier layer because layer 712 blocks certain part of the substrate 710 from being in contact with the conductive path 752." Applicants respectfully disagree.

As illustrated in Figures 7D, 7E, and 7F, and as described at col. 13, lines 9-11, signal line 752 and underlying via 754 extend all the way to the substrate. As illustrated in Figures 7D, 7E, and 7F, fabrication of signal line 752 is accomplished by etching all the way to the substrate. In Figure 7B, signal line 752 (722 in Fig. 7B prior to fill) is fabricated only to first dielectric layer 712 at the same time as power line trench 720 is fabricated because while first and third dielectric layers 712 and 716 are of the same or similar composition, second dielectric layer 714 is of a dissimilar material providing desired etch selectivity and requiring different etching chemistry.

If, contrary to the plain terms of the reference that the disclosed triple-damascene structure is comprised of at least three dielectric layers, it should be clear *what* the first dielectric layer as barrier is serving as a barrier for or against. By way of example, as illustrated and defined in Applicants' specification as filed, "a barrier layer 102 is deposited to protect the copper material 122 from premature oxidation when via holes are etched through overlying dielectric materials to the barrier layer 102" (page 10, lines 8-10). The structure and the purpose of the structure is clearly identified and defined. In the Parikh reference, however, no corresponding definition or illustrated structures exist. Applicants respectfully submit that no such structures exist because first dielectric layer 712 of the Parikh structure is just that: a first dielectric layer of at least three dielectric layers, and not a barrier layer.

Mixing and matching portions or discrete pieces or sections of structures does not teach or disclose the claimed structure. There are certainly barriers, conductive paths, metallization layers, dielectric layers, etc., found in virtually all semiconductor structures, but their existence does not teach or disclose all known semiconductor structures. Applicants are claiming a specific dual damascene structure, and the barrier layer, functioning as a barrier layer, is one feature of the structure. According to the Office, the structure as taught by Parikh in Fig. 7F teach or suggest Applicants' claimed structures including a barrier layer disposed over a substrate, an inorganic dielectric layer disposed over the barrier layer, and a low dielectric constant layer disposed directly over and in direct contact with the inorganic dielectric layer.

Applicants have cited numerous sections of the reference that teach otherwise. A side-by-side comparison of the structures emphasizes the differences in the structures, and supports Applicants' position that the claimed invention as recited in independent claims 21 and 36 is patentable over the reference:

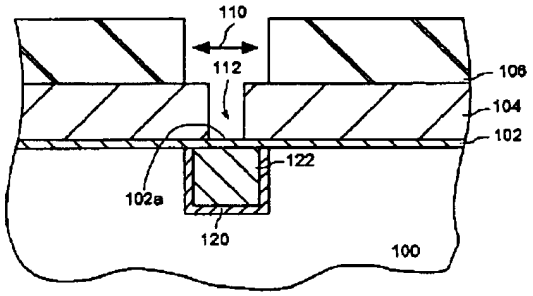

FIG. 5

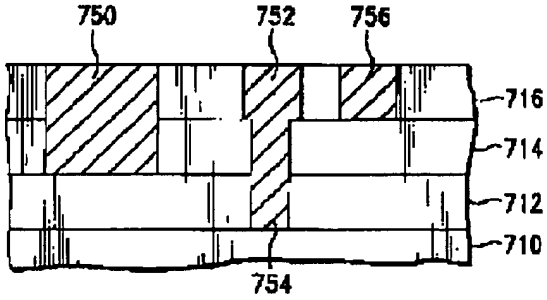

FIG. 7F

Fig. 5 above is Applicants' claimed dual damascene structure. Fig. 7F shows the Parikh triple damascene structure. According to the Office, Applicants' barrier 102 is taught by Parikh's first dielectric layer 712. Applicants submit that no one of ordinary skill in the art would be moved to draw such a conclusion.

For at least the above reasons, Applicants submit that either Parikh alone, or the combination of Parikh with Yu et al. fail to teach or suggest all the claim limitations, and therefore do not render Applicants' independent claims 21 and 36 obvious. Similarly, dependent claims 37-40, each of which depend directly or indirectly from independent claim 36, are likewise patentable over the cited art. Applicants respectfully request that the 35 U.S.C. §103 rejection of claims 21, and 36-40 be withdrawn.

Claims 21, and 31-40 were rejected under 35 U.S.C. §103(a) as being unpatentable over Parikh in view of Applicants' admitted prior art. The rejections are traversed and Applicants request reconsideration.

With respect to Applicants' independent claims 21, 31, and 36, the rejection is essentially the same as that described above in reference to independent claims 21 and 36. In reference to independent claim 31, the rejection is essentially the same, except that Parikh fails to teach a base dielectric over which the barrier is disposed. For at least the same reasons as stated above in reference to independent claims 21 and 36, Applicants submit that claims 21 and 31-40 are patentable over the cited art, and request that these rejections be withdrawn.

Claims 21-23 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,255,735) in view of Applicants' admitted prior art.

Wang et al. disclose a conductive layer (10) over which an etch stop layer (12) has been formed. A first dielectric layer (14) is formed over the etch stop layer (12), and a second dielectric layer (18) is formed over the first dielectric layer (14). The second dielectric layer (18) is a low k dielectric material that is spin-coated on the first dielectric layer (14). Wang et al. describe the first dielectric layer (14) as formed of a low k dielectric material with a k value of less than 4 (see col. 5, lines 32-35), and the second dielectric layer (18) also being comprised of a low k dielectric material (col. 5, lines 55). The second low k dielectric material is disclosed to require a different sensitivity than the low k dielectric material in the first dielectric layer (14) to at least one etchant chemistry (col. 5, lines 60-63), although it is not disclosed that one or the other layer needs to have the lower of the two low k values.

Wang et al., do not disclose an inorganic dielectric layer disposed over a barrier, the inorganic dielectric layer having a dielectric constant of about 4, and a low dielectric constant layer disposed directly over and in direct contact with the inorganic dielectric layer.

The Office asserts that Wang et al. is silent about the inorganic dielectric layer having a dielectric constant of about 4. Applicants respectfully disagree. Wang et al.

explicitly teach a low k dielectric over a low k dielectric (see, for example, the Abstract, col. 5, lines 7-11, col. 6, lines 1-11, col. 8, lines 12-17, etc.). Applicants have specifically recited a k value of about 4 to specifically claim an inorganic dielectric layer that is not a low k dielectric layer.

The Office then asserts that the k value is considered to involve routine optimization and within the level of ordinary skill in the art. Applicants respectfully disagree. While the Office has asserted that the k value of the dielectric material is one of routine optimization, the Office has overlooked that a k value of a dielectric material is of material importance to the formation of a semiconductor device or structure, and to the resulting structure so formed, which is well known in the art. The k value of a dielectric is not merely a parameter of, for example, temperature or concentration, and as is well known in the art, the selection of a low k dielectric or election not to use a low k dielectric defines and determines the material properties and function of the resulting structure or device. Applicants have specifically claimed a k value of the inorganic dielectric layer of about 4 to specifically claim that the inorganic dielectric layer is ***not*** a low k dielectric layer. However, according to the Office, Applicants' admitted prior art can be used to supply the missing ingredient. Using Fig. 1 and page 2 of the specification as filed, the Office asserts that the prior art described by Applicants teaches a k value of the inorganic dielectric layer of about 4. As above, the Office is mixing and matching pieces to attempt to kluge together a coherent whole that seems to be the structure as claimed by Applicants. The structure illustrated in Fig. 1 of Applicants' specification as filed, illustrates the known prior art of a damascene structure having two oxide layers separated by a trench stopping layer 16b. Because the trench stopping layer provides the desired selectivity during etch, the differing material properties of the two oxide layers is not material. Even if the admitted prior art discusses a particular k value for the via layer, a combination with the Wang et al. reference is without motivation.

For at least the above reasons, Applicants submit that the combination of Wang et al. and admitted prior art do not render obvious Applicants' independent claim 21. Dependent claims 22-23, depending directly or indirectly from independent claim 21 are therefore also not rendered obvious. Applicants request the §103 rejection be withdrawn.

Claims 24 and 26-30 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al. in view of Applicants' admitted prior art as applied to claim 23, and further in view of Usami (U.S. Patent No. 6,077,574). Applicants traverse this rejection and request reconsideration.

Applicants respectfully submit that, for at least the reasons that independent claim 21 is patentable as described above, dependent claims 24 and 26-30, each of which depend directly or indirectly from independent claim 21, are likewise patentable. Applicants request that these rejections be withdrawn.

Claims 31-35 were rejected under 35 U.S.C. §103(a) as being unpatentable over Wang et al. in view of Applicants' admitted prior art and Usami. Applicants traverse this rejection and request reconsideration.

Independent claim 31 has been described above. For at least the reasons that Wang et al. fail to render Applicants' independent claim 21 obvious, so too does the Wang et al. reference fail to render Applicants' independent claim 31 obvious. Dependent claims 32-35, each of depend directly or indirectly from independent claim 31 are likewise patentable. Applicants request that these rejections be withdrawn.

Allowable subject matter

Applicants acknowledge independent claim 41 as being indicated to be allowable. New claims 42-46, depending from independent claim 41 are submitted for examination. Support for the new claims is found in originally filed claims, and Applicants' specification as filed on pages 13-14.

Further, new independent claim 47, and dependent claims 48-54 are submitted for examination. Support for these claims is the same as that for claims 42-46.

In view of the foregoing, Applicants respectfully request reconsideration of claims 21-24, and 26-41, and examination of new claims 42-54. Applicants submit that all claims are in condition for allowance. Accordingly, a notice of allowance is

respectfully requested. If Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6905. If any additional fees are due in connection with filing this amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM1P106D). A copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
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